



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,792	05/28/2004	Chao-Ping Chuang	AMIP0027USA	3791
27765	7590	12/12/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			MCLEAN MAYO, KIMBERLY N	
			ART UNIT	PAPER NUMBER
			2187	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/709,792

Applicant(s)

CHUANG ET AL.

Examiner

Kimberly N. McLean-Mayo

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-9 and 12-16 is/are rejected.
- 7) ☒ Claim(s) 3,4,10 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The enclosed detailed action is in response to the Priority Papers and the Application submitted on May 28, 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-2, 5-9 and 12-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Park et al. (PGPUB: US 2005/0052922; KR – 2003-18963).

Regarding claim 1, Park discloses a memory device comprising a plurality of memory units each corresponding to an address for recording data (memory cells; section 0022); an interface circuit for receiving address information (logic coupled to the address generator which receives an external address; section 0044; column 2); an address calculation module connected to the interface circuit for providing a first address according to the address information (Figure 1, Reference 200; section 0027; page 3); an address buffer connected to the address calculation module for receiving and storing addresses provided by the address calculation module (logic within the decoder which stores the address for decoding; section 0044; column 2), wherein the address calculation module is capable of generating and providing a second address different from the first address according to the address information after the address buffer stores the first address (sections 0046; 0027, page 3); and a decoding module connected to the address buffer

Art Unit: 2187

for enabling each memory unit corresponding to the first address to output its data when the address buffer stores the first address (Figure 1, References 140 and 160; section 0022), the address calculation module capable of providing the second address after each memory unit corresponding to the first address outputs its data (section 0046), the address buffer being capable of storing the second address provided by the address calculation module, and the decoding module being capable of enabling each memory unit corresponding to the second address to output its data (sections 0022, 0027 and 0044).

Regarding claim 2, Park discloses wherein at least two of the plurality of memory units correspond to the same address (all of the memory cells constituting a sector correspond to the same address; section 0022); wherein the memory device further comprises at least one output buffer each connected to each memory unit corresponding to the same address, when each memory unit corresponding to the same address synchronously outputs its data, the output buffer is capable of storing the output data provided by each memory unit and providing data as output of the memory device for each memory unit at different times in turn (Figure 1, Reference 170; sections 0025 and 0037).

Regarding claim 5, the output buffer is further connected to the interface circuit and provides output data for each memory unit in turn through the bus of the interface circuit set for receiving the address information (Figure 1, References 170 and 230).

Art Unit: 2187

Regarding claim 6, Park discloses the memory device is a non-volatile memory (Figure 1, Reference 100; flash memory device);

Regarding claim 7, Park discloses the address calculation module calculates the second address by progressively increasing the addresses from the first address (section 0027, page 3; section 0046).

Regarding claim 8, Park discloses the plurality of memory units are arrayed in a matrix and the decoding module comprises a column decoder and a row decoder (section 0022).

Regarding claim 9, Park discloses a plurality of memory units each corresponding to an address for recording data (memory cells; section 0022), wherein at least two memory units are corresponding to the same address (all of the memory cells constituting a sector correspond to the same address; section 0022); a decoding module capable of receiving an address and enabling each memory unit corresponding to the address to output its data (Figure 1, References 140 and 160; section 0022); and at least one output buffer each connected to memory units corresponding to the same address, when the memory units corresponding to the same address output their data synchronously, the output buffer is capable of storing data provided by each memory unit and at different times providing data provided by each memory unit in turn for being output of the memory device (Figure 1, Reference 170; sections 0025 and 0037).

Claim 12 is rejected for the same rationale applied to claim 1 above.

Art Unit: 2187

Claim 13 is rejected for the same rationale applied to claim 5 above.

Claim 14 is rejected for the same rationale applied to claim 7 above.

Claim 15 is rejected for the same rationale applied to claim 6 above.

Claim 16 is rejected for the same rationale applied to claim 8 above.

Allowable Subject Matter

4. Claims 3-4 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran et al. PGPUB : US 2005/0081014 – burst operations in a nonvolatile memory

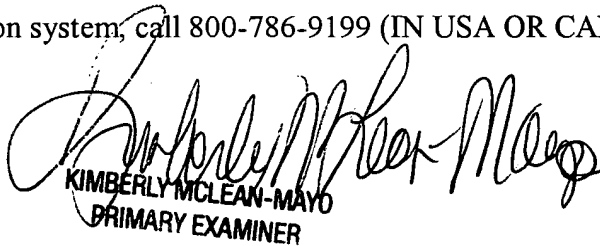
Kim USPN: 6,134,180 – burst read operations in a memory device.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

Art Unit: 2187

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

November 9, 2006